

VP-70 SERVICE NOTES

First Edition

SPECIFICATIONS

Input Level/Impedance	: Unbalanced	-50dBm/1MΩ
		-10dBm/1MΩ
		+4dBm/1MΩ
	: Balanced	-50dBm/600Ω
		-10dBm/600Ω
		+4dBm/600Ω
Output Level/Impedance	: 0dBm/1.2KΩ	
Frequency Response	: 20Hz – 30KHz	dB (Direct)
	: 35Hz – 15KHz	dB (Effect)
S/N Ratio	: 89.2dB (Direct)	
	: 68.6dB (Effect)	
	[JIS-A, SHIFT ON : U1–U4 set at -12]	
Power Consumption	: 17W @100V	
	: 20W @117V/220V/240V	
Dimensions	: 482 (W) x 276 (D) x 44 (H) mm	
	: 19 (W) x 10-7/8 (D) x 1-3/4 (H) in.	
Weight	: 4kg	8 lb. 13 oz.
Accessory	Connection Cable LP-25 (PART No. 22430675S0)	

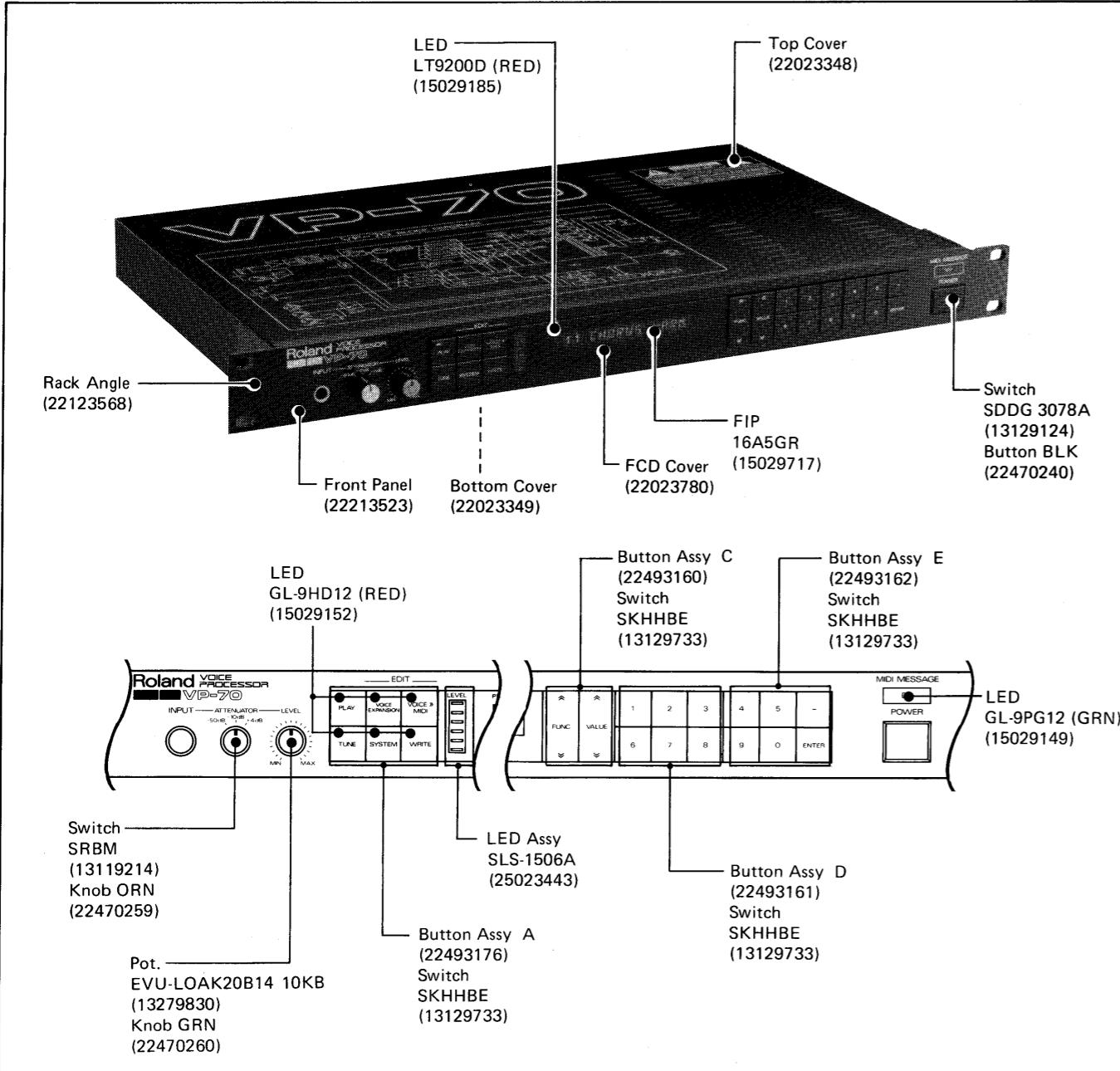
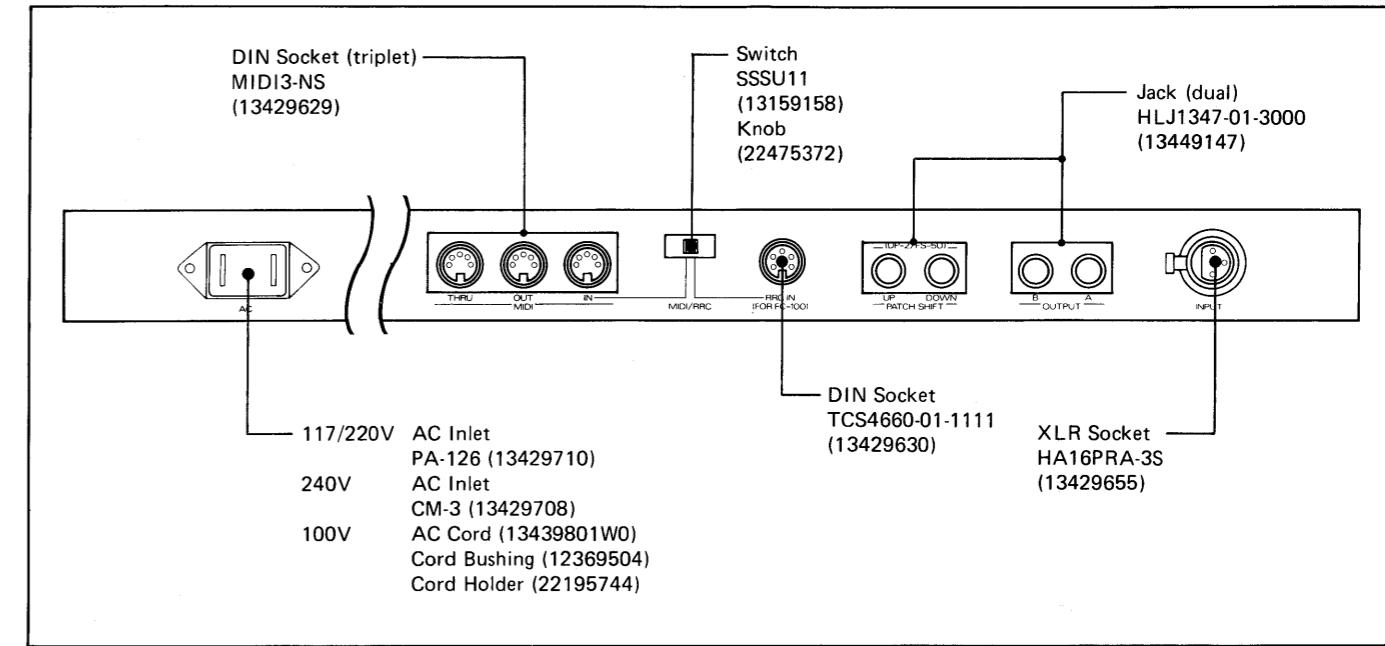
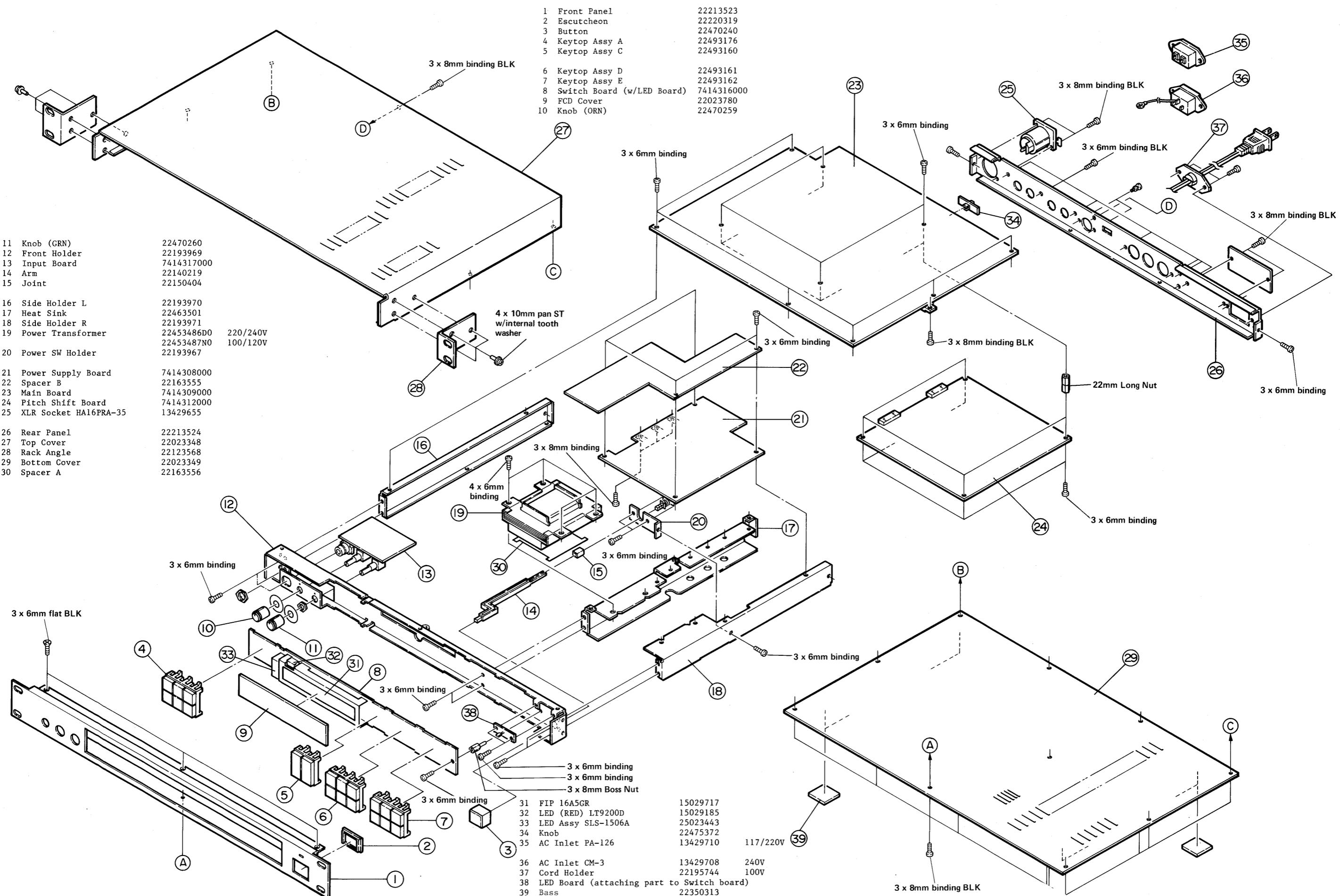


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EXPLODED VIEW**A****B****C****D****E****F****G****H****I****J****K****L****M****N****O****P****Q****R****S****T****U**

CAUTION

To EP-ROMs A and B (PART No. 15179805, 15179806), no other ICs than specified below cannot be applied.

Mitsubishi M5M27C128K-2

Program data copied into the other brands' or different type will not work on the VP-70.

注意事項

EP-ROM A及びB(PART No.15179805, 15179806)は指定品であり、以下に示したもののみ使用できます。

三菱電気製 M5M27C128K-2

メーカー又は製番の異なるEP-ROMに、プログラムデータをコピーし、本製品に使用した場合、正常に動作しないことがあります。

PARTS LIST**CASING**

22023348	Top Cover
22023349	Bottom Cover
22213523	Front Panel
22213524	Rear Panel
22193969	Front Holder
22193970	Side Holder (Left)
22193971	Side Holder (Right)
22123568	Rack Angle

KNOB, BUTTON

22470259	Knob ORN
22470260	Knob GRN
22493176	Keytop Assy. A
	PLAY, TUNE, VOICE EXPANSION, TUNE, SYSTEM, WRITE
22493160	Keytop Assy. C
	FUNC, VALUE
22493161	Keytop Assy. D
	1, 2, 3, 6, 7, 8
22493162	Keytop Assy. E
	4, 5, 9, 0, -, ENTER
22470240	Button BLK
	POWER

SWITCH

13129124	SDDG 3078A (Push)	POWER
13159158	SSSU 11 (Slide)	MIDI/RRC
13129733	SKHHBE (Tact)	
13119214	SRBM	ATT

JACK, SOCKET

13449147	HLJ1347-01-3000 (Dual)	PATCH SHIFT, OUTPUT
13429630	TCS4660-01-1111 (6P DIN)	RRC IN
13429629	MIDI3-NS (Triplet)	MIDI
13449149	YKB21-5011	INPUT
13429655	HA16PRA-3S	XLR Socket

POWER TRANSFORMER

22453487NO	100V/120V
22453486DO	220V/240V

COIL

12449251	244-251	DC-DC Converter
12449244	SC-02-15E	Line Filter Coil

PCB ASSY

7414309000	Main Board	(pcb 22923475)
7414312000	Pitch Shift Board	(pcb 22923476)
7414316000	Switch Board w/LED Board	(pcb 22923477)
7414317000	Input Board	(pcb 22923480)
7414308000	Power Supply Board	(pcb 22923478)

POTENTIOMETER

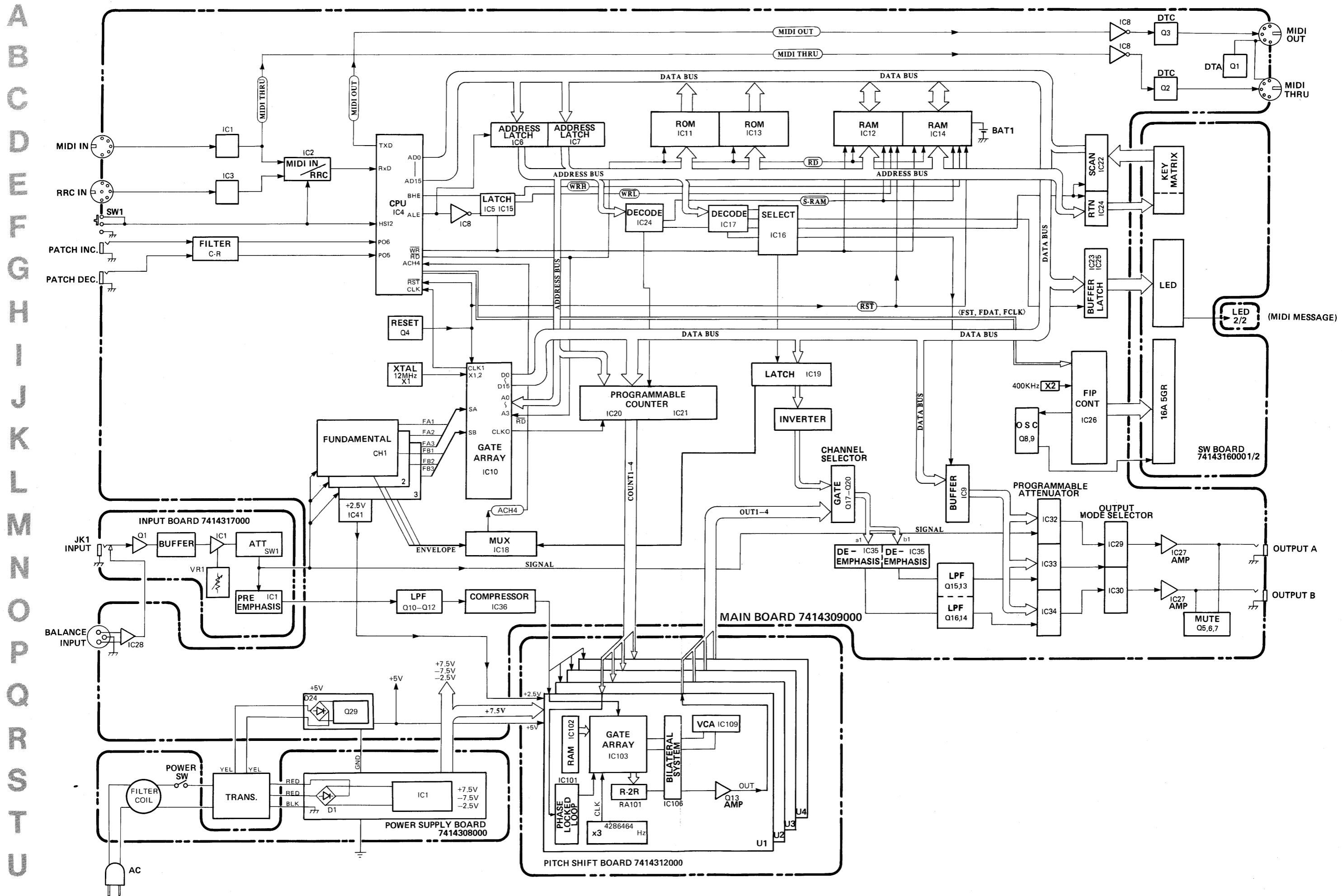
13279830	EVU-LOAK20B14	LEVEL
13299195	EVND4AA00B14	10KB MAIN BOARD
13299193	EVND4AA00B54	50KB MAIN BOARD

IC			
15179246	i8095	CPU	
15229845	MSM75H016	Gate Array	
15179201	μPD7537C-014	FIP Controller	
15179334	TC5564PL-20	S-RAM	
15179805	M5M27C128K-2	EP-ROM A	
15179806	M5M27C128K-2	EP-ROM B	
		No substitutive brand or types for EP-ROMs A or B as a replacement. EP-ROM A,Bは指定品です。交換時には、必ず同一品を用いて下さい。	
15179110N0	μPD8253C-2	Programmable Counter	
15169340H1	HD74LS347	Octal Transparent Latch	
15169319H0	HD74LS139	Dual 2 to 4 Demultiplexers	
15159113H0	HD14051BP	Single 8-Channel Multiplexer/Demultiplexer	
15159129H0	HD14053BP	Triple 2-Channel Multiplexer/Demultiplexer	
15169515	TC74HC00P	Quad 2-Input NAND Gate	
15169514	TC74HC04P	Hex Inverter	
15169549T0	TC74HC32P	Quad 2-Input OR Gate	
15169513	TC74HC74P	Dual D Flip-Flop with Preset and Clear	
15169550T0	TC74HC138P	3-to-8 Line Decoder	
15169551T0	TC74HC174P	Hex D Flip-Flop with Clear	
15169552T0	TC74HC245P	Octal 3 STATE Transceiver	
15169553	TC74HC373P	3 STATE Octal D-type Latch	
15169554T0	TC74HC374P	3 STATE Octal D-type Flip-Flop	
15219108	NE570N	COMPANDOR	
15229843	M74007BOS-0001	GATE ARRAY	
15179381	M5M4416P-15	D-RAM	
15159111H0	HD14046BP	Phase-Locked Loop	
15159115H0	HD14066BP	Quad Bilateral Switch	
15219186	M5207L-05	VCA	
15189171	M5218P	OP Amp	
15189111J1	NJM311	Precision Voltage Comparator	
15189152	NJM5534	OP Amp	
15189136	M5218L	OP Amp	
15229706	TLP-552	Optoisolator	
1599137	AN7805F	+5 Voltage Regulator	
15219139	PST518	RESET	
TRANSISTOR			
15119814	2SB1015		
15129827	2SD1406		
15119111	2SA970GR		
15129120	2SC2240GR		
15129107	2SC945		
15129613	2SD1207S		
15119134	2SA933		
15129152	2SC2878A		
15119141	DTA-114ES	w/built-in bias resistors	
15129164	DTC-114ES	w/built-in bias resistors	
15139121	2SK117GR	FET	
DIODE			
15019126	1SS-133		
15019143	1S-116		
15019323	04AZ9.1X		
15019324	04AZ39X		
15019324	4D4B41	Rectifier Bridge	
15019243	1B4B1	Rectifier Bridge	
15029185	LT9200D	LED (RED)	
15029152	GL-9HD12	LED (RED)	
15029149	GL-9PG12	LED (GRN)	
25023443	SLS-1506A	LED Assy	
FUSE			
41015158	SD6 315mA	100V/120V	
12559539	CEE T125mA	220V/240V	
AC CORD			
13439812F0	JC-704-J01	120V	
13439813F0	EC-210-J06	220V	
23495110	5722-660-4606	240VE	
13439814F0	SC-415-J06	240VA	
RESISTOR			
13919308	RMLS 6-103J	10K X 6	
13919310	RMLS 8-103J	10K X 8	
13919172	RKM10L502F		
12559810	ERQ-16NK1R5E	Fuse Resistor	
FIP, FCD COVER			
15029717	16A5GR	FIP	
22023780	FCD Cover		

CAPACITOR			
13629155J0	SR16VB2200	2200/16V	
13529104	DE7150F472MVA1		
13659205	ECEA1CSS332	3300/16V	
13619706N0	CS15E1VR68K1S	0.68/35V T	
13619703N0	CS15E1VR221S	0.22/35V T	
CRYSTAL			
12389765	TQC-226A-6R	12MHz	
12389738	CSB400P	400kHz	
12389757	HC-49/U	4.2	

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

BLOCK DIAGRAM



CIRCUIT DESCRIPTIONS

GENERAL DESCRIPTION

The main features of the VP-70:

Voice to MIDI

Determines the pitch and dynamics of the incoming voice (single) and converts them into a suite of MIDI messages containing such information on Note, Volume, Bender and After Touch.

Harmonizing

Pitch shifts the input voice by a predetermined degree.

Pitch Follow

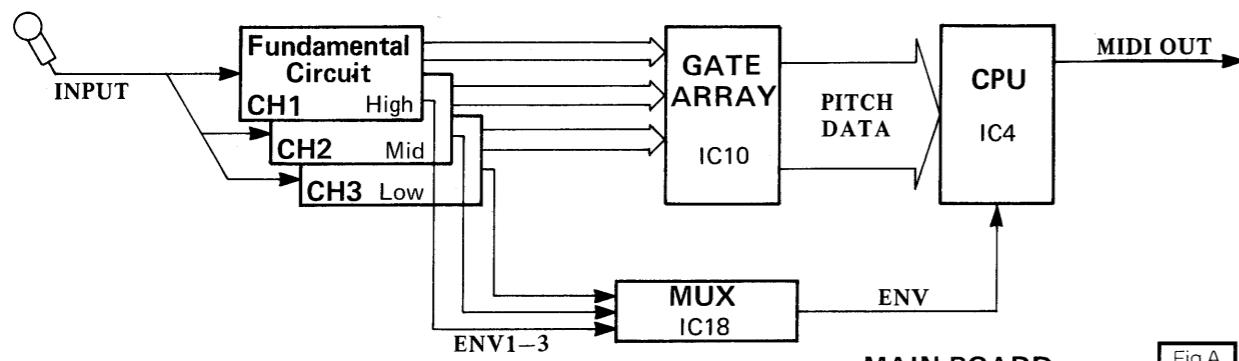
Reproduces a voice at a fixed note irrespective of input signal pitch.

CONTROL SECTION

The main CPU IC4 8095 (main board) manages the following functions and devices on the main board.

- * Transferring of MIDI messages
- * Reception of RRC signal
- * Gate Array IC10 MSM75H016
- * FIP Controller IC26 (CPU) μPD7537C-014
- * Programmable Counters ICs 20 and 21 82C53

DETAILED DESCRIPTION FUNDAMENTAL CIRCUIT (CH1-CH3)



The fundamental circuit consists of three channels connected in parallel. The three channels share audio spectrum; each being assigned with different frequency range, Low, Mid or High, respectively. When a single input sound is applied, each channel determines the fundamental of the sound. Then a channel generates two kind of pulses whose duty cycle equal the period from the first positive peak to the second positive peak and from the first negative peak to the second negative peak, respectively, of the fundamental. Each channel also determines the envelope of the input voice and feeds the contour amount to multiplexer IC18.

回路解説

概要

VP-70の主な機能は、次の通りです。

- ・入力された単音の音声信号からピッチ及びダイナミクスを検出し、MIDIメッセージ（ノート情報、ボリューム情報、ベンダー情報、アフタータッチ情報）に変換する。[VOICE→MIDI機能]
- ・入力された音声を指定されたシフト量を基にピッチシフトする。[ハーモナイズ機能]
- ・入力された音声を指定した一定のキーの高さで発音させる。[ピッチフォロー機能]

制御部

メインCPUには8095 (IC4)が使用されており、以下のものを制御しています。

- MIDIメッセージの送受信
- RRC信号の受信
- ゲートアレイ MSM75H016 (IC10)
- FIP用CPU μPD7537C-014 (IC26)
- プログラマブルカウンター 82C53 (IC20, 21)

詳細 音声信号(単音)→変換→MIDIメッセージ

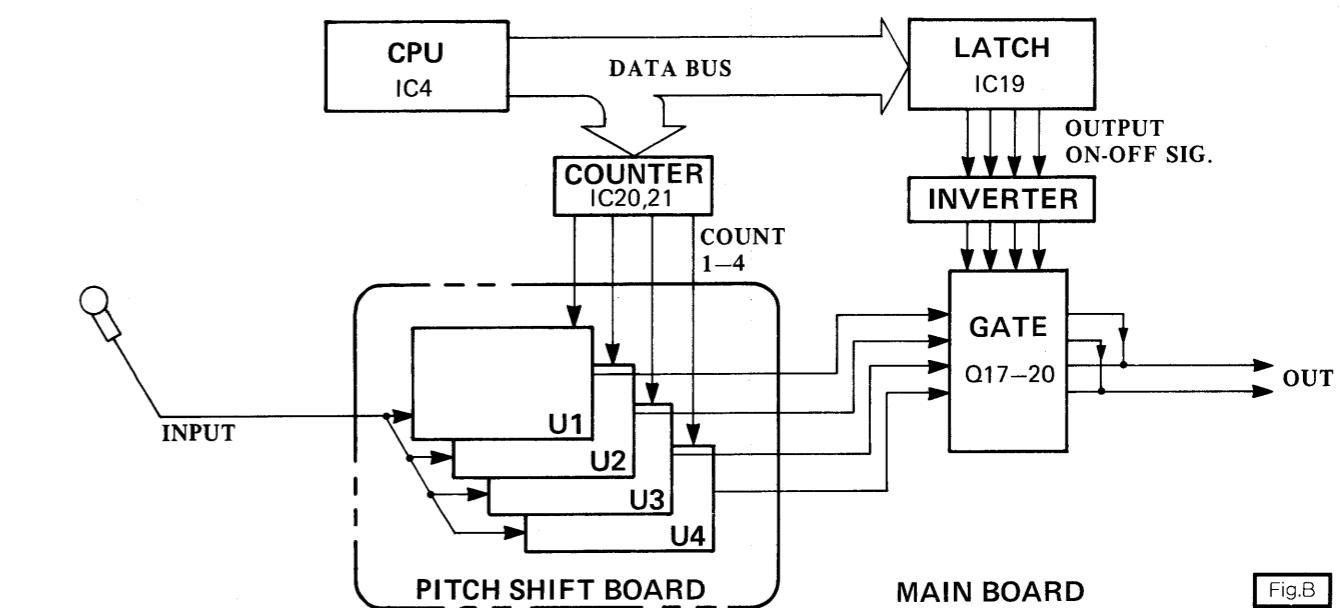
GATE ARRAY (IC10)

The gate array reads the pulses from the fundamental circuit and selects among them the most appropriate ones: since three channels (in the fundamental circuit) have different filtering characteristics, it is easier for the gate array to choose the best. IC10 converts the selected pulses into a pitch data and sends it to the CPU IC4.

CPU (IC4)

The CPU prepares and transmits MIDI messages based on the pitch data from the gate array IC10 and envelope signal from the MUX IC18 (CPU first converts analog envelope signal into digital format at internal A/D converter).

PITCH SHIFT (U1-U4)



GATE ARRAY (IC10)では、入力された音声信号（単音）に応じて（CH1-3の）どのFundamental回路から最良のパルスデータを得る事ができるのかを判断し、その経路からパルスデータを読み込みます。そして読み込んだパルスデータをピッチデータに変換しCPU (IC4)に送ります。

CPU (IC4)はGATE ARRAY (IC10)から送られてくるピッチデータ及びMUX (IC18)から送られてくるエンベロープ信号を基にMIDIメッセージを作り、送信します。

ピッチシフト

Input audio is also routed to Pitch Shift board where the signal is applied to four pitch shift units of the same configuration. The data determining the amount of pitch shift are fed to programmable counters ICs 20 and 21 via the CPU data bus. The CPU has derived the date from patch data or external MIDI Note On message.

The counters generate four clocks at different frequencies or at the same frequency, depending on the mode selected; then pass them onto pitch shift units U1-U4.

入力された音声信号はピッチシフトユニット (U1~U4) へ入力されます。

(U1~U4は全て同一回路構成)

CPU (IC4)はパッチデータまたは外部からのMIDIノート情報に応じたピッチシフト量のデータを、データバスを通じてプログラマブルカウンター (IC20, 21)へ送ります。カウンターはこのデータ (ピッチシフト量) をクロックの形態に変換し、各ユニット (U1~U4)へ送ります。

各ピッチシフトユニット (U1~U4)は、カウンター (IC20, 21)からのクロックの周波数に基づき入力された音声信号を目的の音程に変化させ、ゲート回路 (Q17-20)へ送ります。

音声信号(単音)は並列接続された3つのFundamental回路(3系統)に入力されます。

各Fundamental回路では音声信号(単音)の基本成分を検出し、正信号のピーク間、負信号のピーク間をパルス化し、ピッチデータとしてGATE ARRAY (IC10)へ送ります。また、音声信号(単音)のエンベロープ成分も検出しておらず、MUX (IC18)を介してCPU (IC4)内のA/Dコンバータに読み込まれます。

Fundamental回路 (CH1-3)はオーディオ帯域をLow, Mid, Highに分割したうちの1帯域を1系統ずつ受け持っており、それぞれ異なるFilter特性を有しています。

PITCH SHIFT UNITS (U1-U4)

The following description takes U1 as a representative since four units work with the same circuit configuration.

An input signal passing through S/H circuit (IC107) is converted to the digital equivalent by the comparator (IC105) and the gate array (IC102) which writes the converted data into the RAM. (Fig. 1.) The gate array reads RAM stored data twice from different memory locations by the time next writing cycle starts. Two data are converted into analog voltage at RA101 ([B] and [C]) and then routed to the dedicated VCA, IC109, before being mixed. (Fig. 3.)

This process can well be analogized with a tape recorder having an additional playback head. (Fig. 2.) In Fig. 2 the tape loop stands for a RAM, the recording head (RH) for writing and the playback heads (PH) for reading.

The RH and RHs travel in the same direction along the tape loop which does not run.

Suppose that the two PHs (A and B) run at a rate twice that of the RH, the tone of the played back sounds is one octave higher than the recorded one. The pitch is lowered by one octave than the original when played back at half the recording speed.

NOISE ELIMINATION

The recorded signals on both sides of the RH gap are out of phase to each other — the degree of phase difference depends on the tape length, signal frequency and the time it takes for the RH to revolve the entire tape loop. Therefore, a phase transient occurs at a PH output at every overlap of RH and PH when PHs and RH travel at different speeds, resulting in noise components to be heard.

The two PH configuration overcomes this problem. The two heads are switched to pick up only the signal from a tape location far away off the RH.

In the actual application the control signals [D] and [E] (Fig. 3) cut off respective VCA, IC109, as the writing address and the reading address become close. Note that the address span between the first and the second reading remains constant regardless of reading cycle speed. The outputs from the two VCAs are combined to form [F]. If the phase difference between the two signals ([B] and [C]) becomes more than 90 degrees (Fig. 3 [F])

ピッチシフトユニットについて

各ピッチシフトユニット(U1~U4)の回路構成は全く同一ですのでU1を例にとり説明します。

Fig. 1 のように入力波形 [A] は S / H 回路 (IC107) を経て、コンパレータ (IC105), ゲートアレイ (IC102) で A / D 交換されます。ゲートアレイは A / D 交換されたデータを RAM に書込んでゆくと同時に既に RAM に書き込まれているデータを一定の間隔で 2 回読み出してゆき、D / A コンバータ (RA101) を経て、波形 [B], [C] を発生します (Fig. 3 参照)。この原理をテープレコーダーに置き換えて説明します (Fig. 2 参照)。テープを RAM, RAM への書き込みを録音ヘッド (RH)、読み出しを再生ヘッド (PH) に対応させます。静止したエンドレステープ上で、対称位置にある 2 つの PH ヘッド A, B ならびに RH ヘッドが同一方向に回転しているとします。今、PH のスピードを RH の 2 倍にすると、再生音のピッチは原音の 2 倍に、スピードを 1/2 にするとピッチも 1/2 となります。

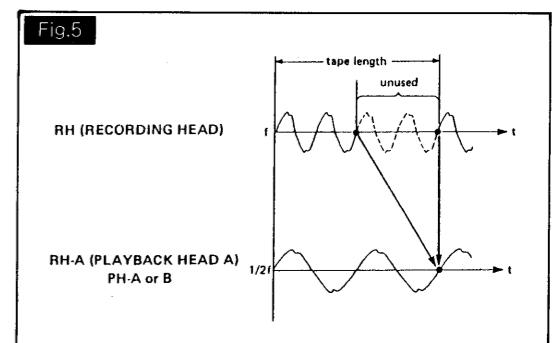
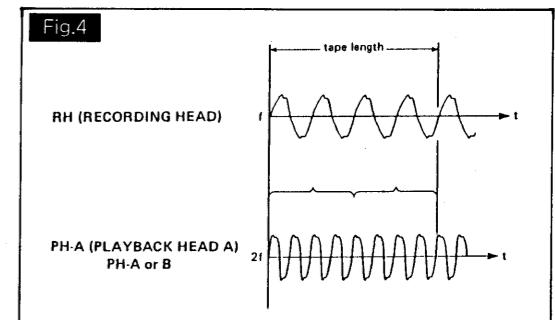
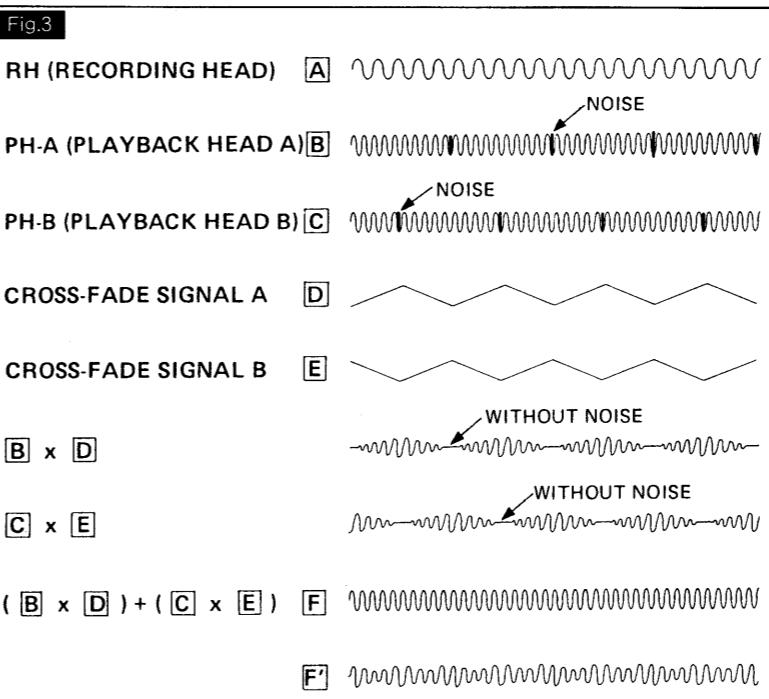
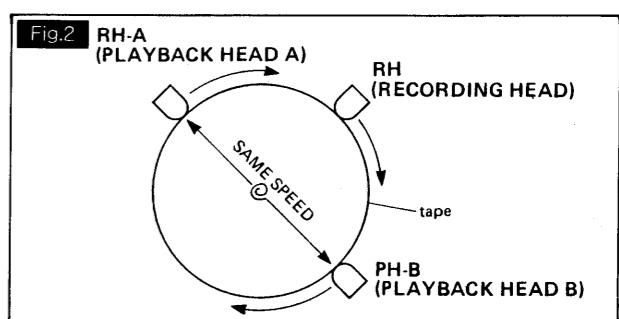
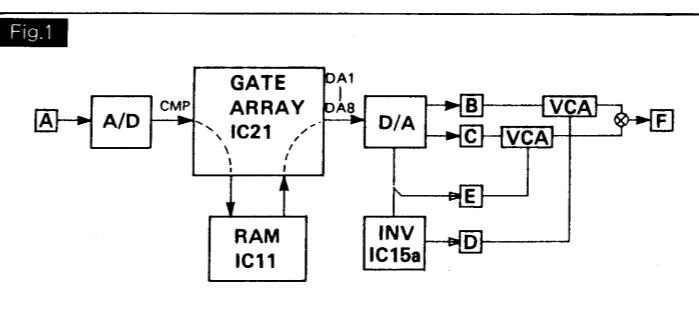
PLAYED BACK SOUND DURATION

The duration of a played back sound will vary as its pitch shifts from the original sound. With this two head configuration the same portion of a recorded sound* is reproduced twice when PHs run at double the RH speed (Fig. 4). Inversely, when PHs are slowed to half the RH speed, they skip half of the recorded portion per recording loop (Fig. 5). Similar compromise should take place at various playback speeds to maintain the both pitch equal.

* Can safely be said so because the time elapse from the first reading is negligible when compared with period of the sounds.

再生音の長さ

通常のテープ式エコー等では、再生音のピッチが原音からずれるに応じて、音の長さが変化します。本方式では、ピッチが 2 倍になった時には PH が RH の 2 倍のスピードでまわり同一音（とみなして差支えない）を 2 度再生しますし (Fig. 4)、逆に 1/2 になった時には RH がテープを 2 周する間に各周の録音 RH 信号の半分づつのみを再生するので (Fig. 5)、音の再生時間長は抱わらず常に一定となります。



DETERMINING ROM VERSION NUMBER

The display reads current ROM version number when power is applied while holding [PLAY], [VOICE >], [MIDI] and [SYSTEM] buttons; and keeps the reading as long as these buttons are held down.

CAUTION

Releasing the three buttons changes the reading to sign-on message in the normal play mode. This is false reading and the unit does not change mode: Twiddling the unit without first turning off and repowering may cause malfunctioning.

ROMバージョンの確認方法

- [PLAY], [VOICE >], [MIDI], [SYSTEM] のボタンを同時に押しながら電源を入れる。
- バージョン確認モードに入り、上記ボタンを押している間、ディスプレイに "VER X.XX" と表示します。

注意

ボタンを離すとディスプレイ表示は通常モードと同じ状態になりますが、モードそのものは切り換わっていません。

そのまま使用していると正常に動作しないことがあります。従って通常に使用する場合は一旦電源を切って下さい。

ADJUSTMENT

Set ATT to -10dB and LEVEL to the center. Connect scope to TP1 (of Main Board).

1. BIAS SET

- 1-1. Keep INPUTs (balanced and unbalanced) disengaged.
- 1-2. Adjust VR2 for a 2.5V reading on the screen. Fig. A

2. OFFSET

- 2-1. Feed a 1KHz sinewave from audio generator (AG) to INPUT (unbalanced).
- 2-2. Adjust AG output level so that all yellow LEDs on the VP-70 level meter are lit and red one is on the onset of lighting.
- 2-3. Adjust VR1 for a 3Vp-p reading on the scope. Fig. B

調整仕様

TP-1にオシロスコープを接続し、ATTツマミを -10 dB, LEVEL ツマミを中央にセットする。

1. バイアス セット

- 1-1. INPUT端子（アンバランス、バランス共）を開放にする。
- 1-2. オシロスコープの波形が +2.5 V になるように VR 2 を調整する。（Fig. A参照）

2. オフ セット

- 2-1. INPUTジャック（アンバランス）に発振器を接続する。
- 2-2. 1 KHz の正弦波を入力し、VP-70本体のレベルメータが黄色の範囲から赤に移り変わる直前に発振器の出力を調整する。
- 2-3. オシロスコープの波形が 3 Vp-p になるように VR 1 を調整する。（Fig. B参照）

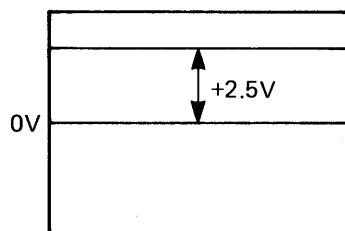


Fig.A

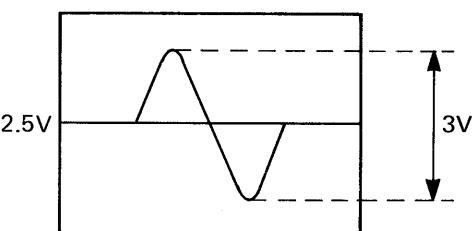


Fig.B

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

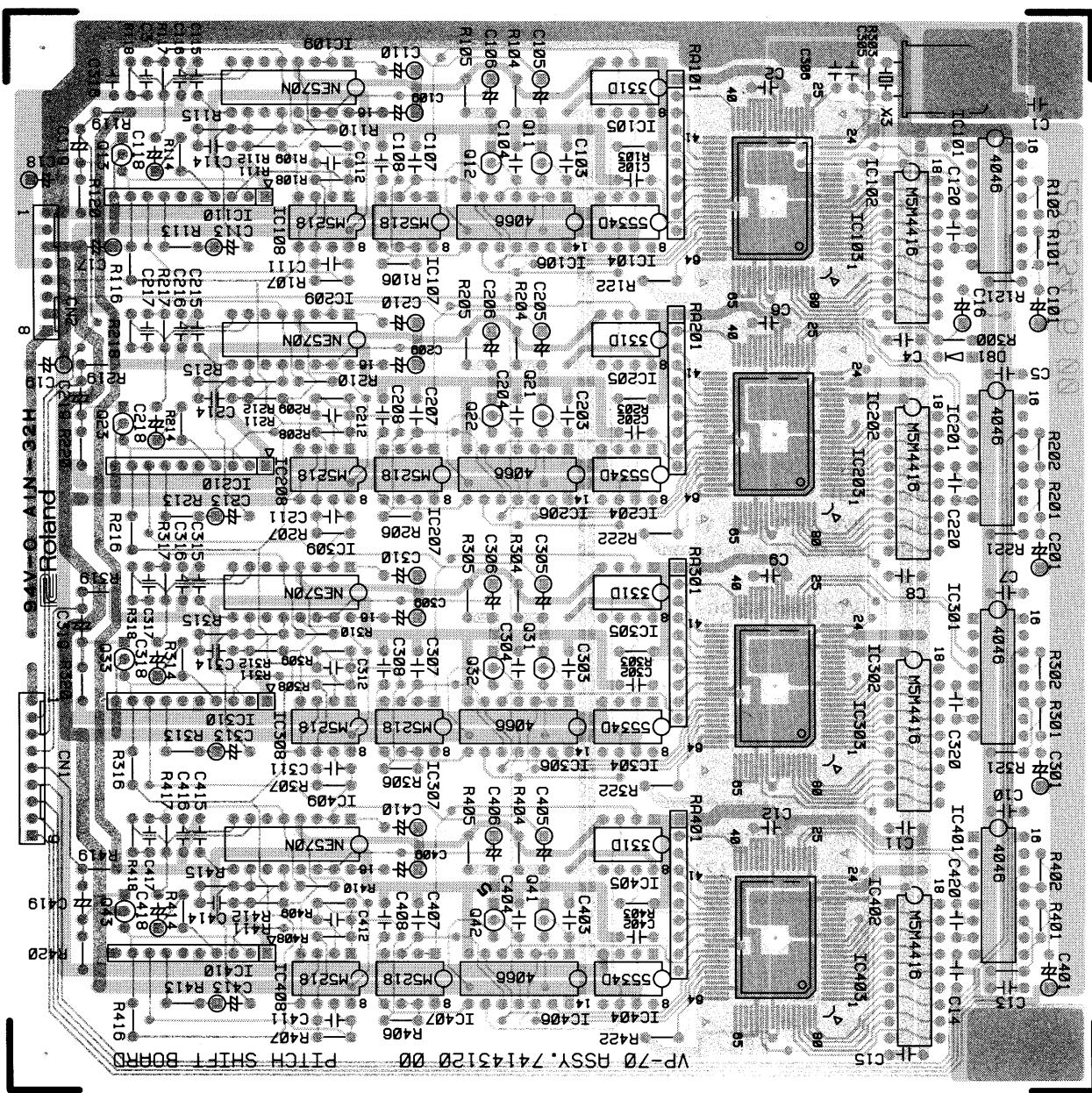
A
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M
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P
Q
R
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T
U
V
W
X
Y
Z

PITCH SHIFT BOARD

ASSY 7414312000

(pcb 2292347600)

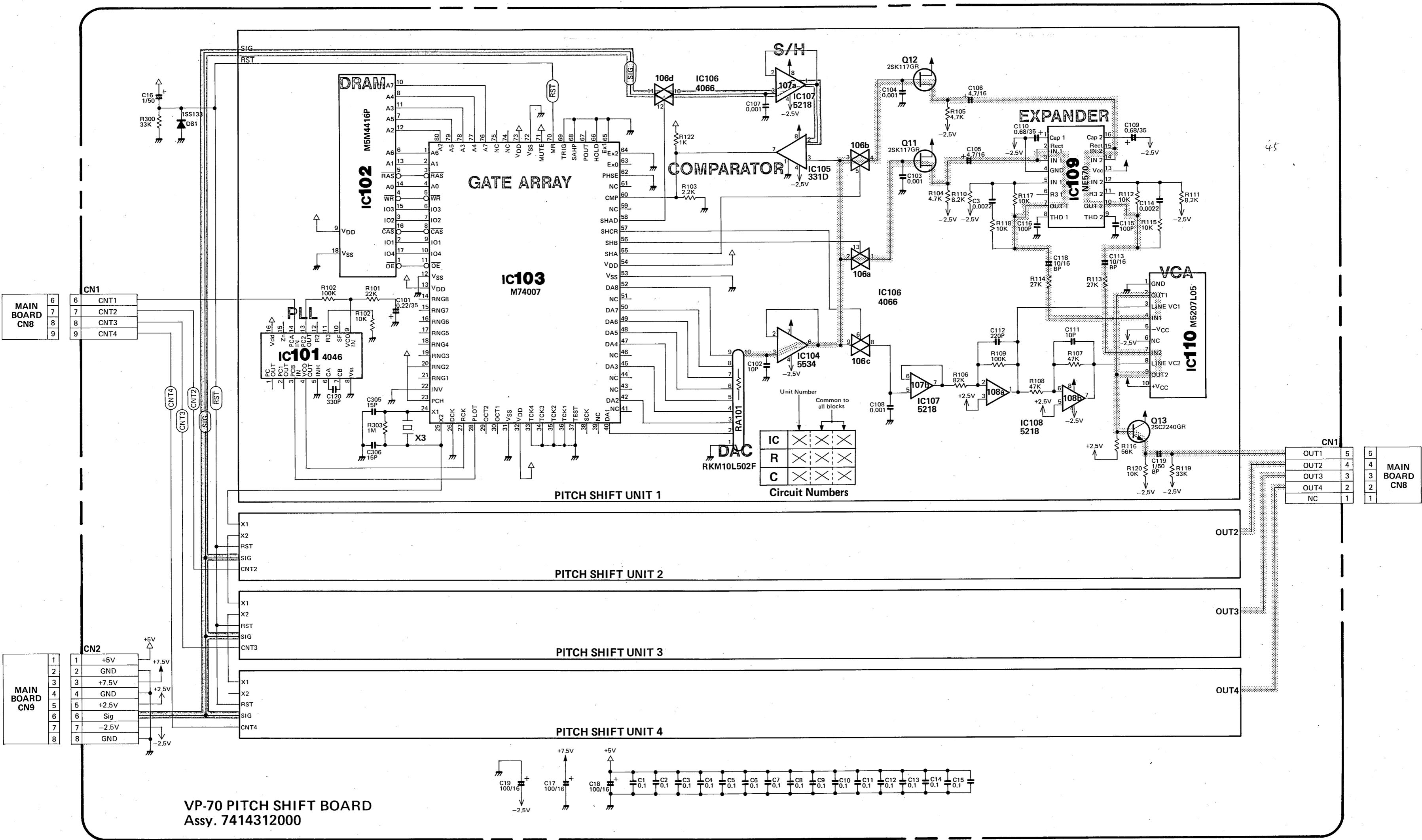
View from component side



VP-70 ASSY.74143120 00 PITCH SHIFT BOARD

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49

CIRCUIT DIAGRAM

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
ZVP-70 PITCH SHIFT BOARD
Assy. 7414312000

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

A
B
C
D
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K
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Q
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X
Y**MAIN BOARD**
ASSY 7414309000
(pcb 2292347500)**ADVARSEL!**

Lithiumbatteri. Eksplorationsfare.
Udskiftning må kun foretages af en sagkyndig,
og som beskrevet i servicemanual.

Lithium batteri må kun udskiftes med samme type
og fabrikat.

ADVARSEL!

Lithiumbatteri. Fare for eksploration.
Ma bare skiftes av kvalifisert tekniker som
beskrevet i servicemanualen.

Lithium batteri må kun utskiftes med samme type
og fabrikat.

VARNING !

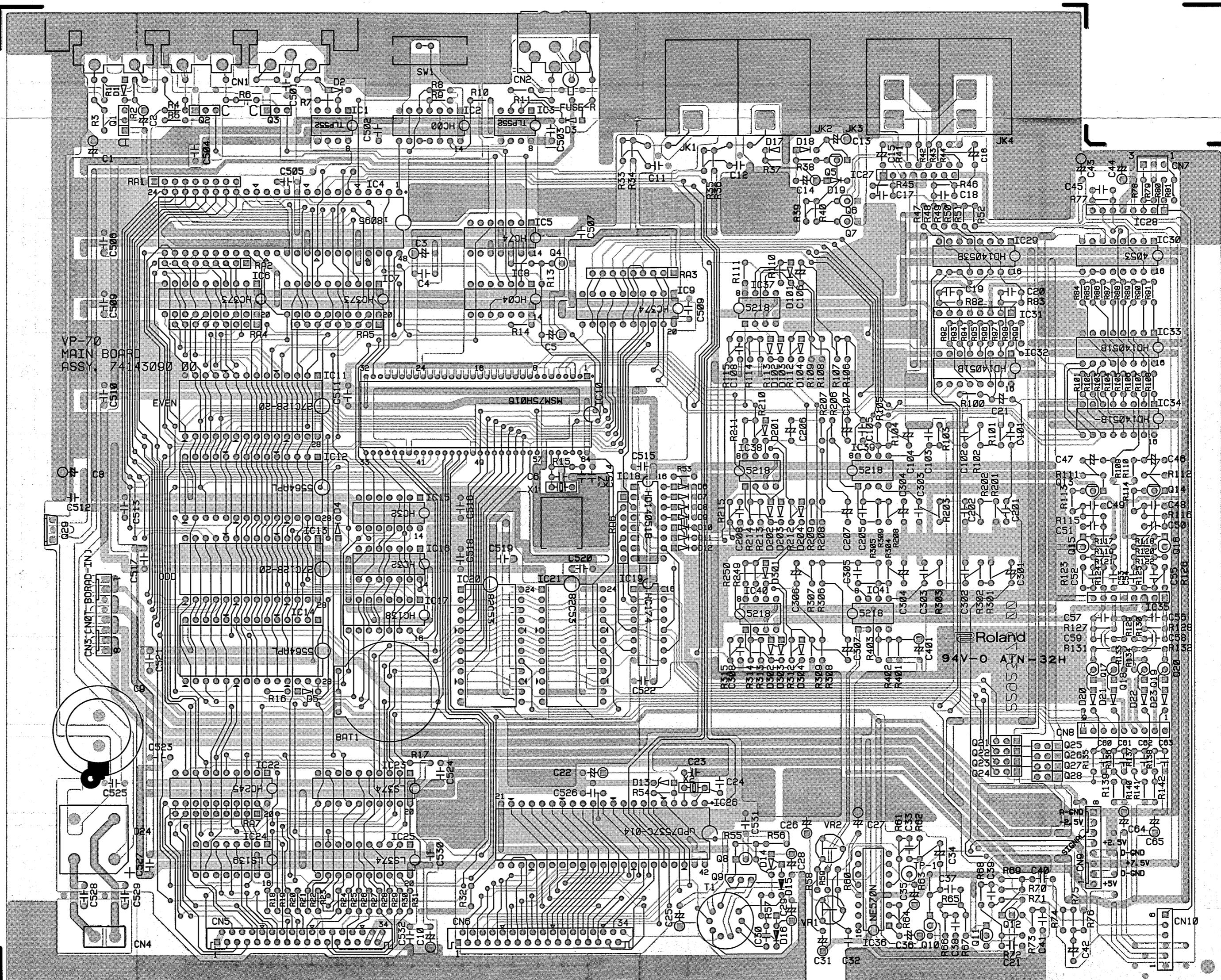
Lithiumbatteri. Explosionsrisk.
Far endast bytas av behörig servicetekniker.
Se instruktioner i servicemanualen.

Lithium batteri för endast ersättas med samma typ
och fabrikat.

VAROITUS!

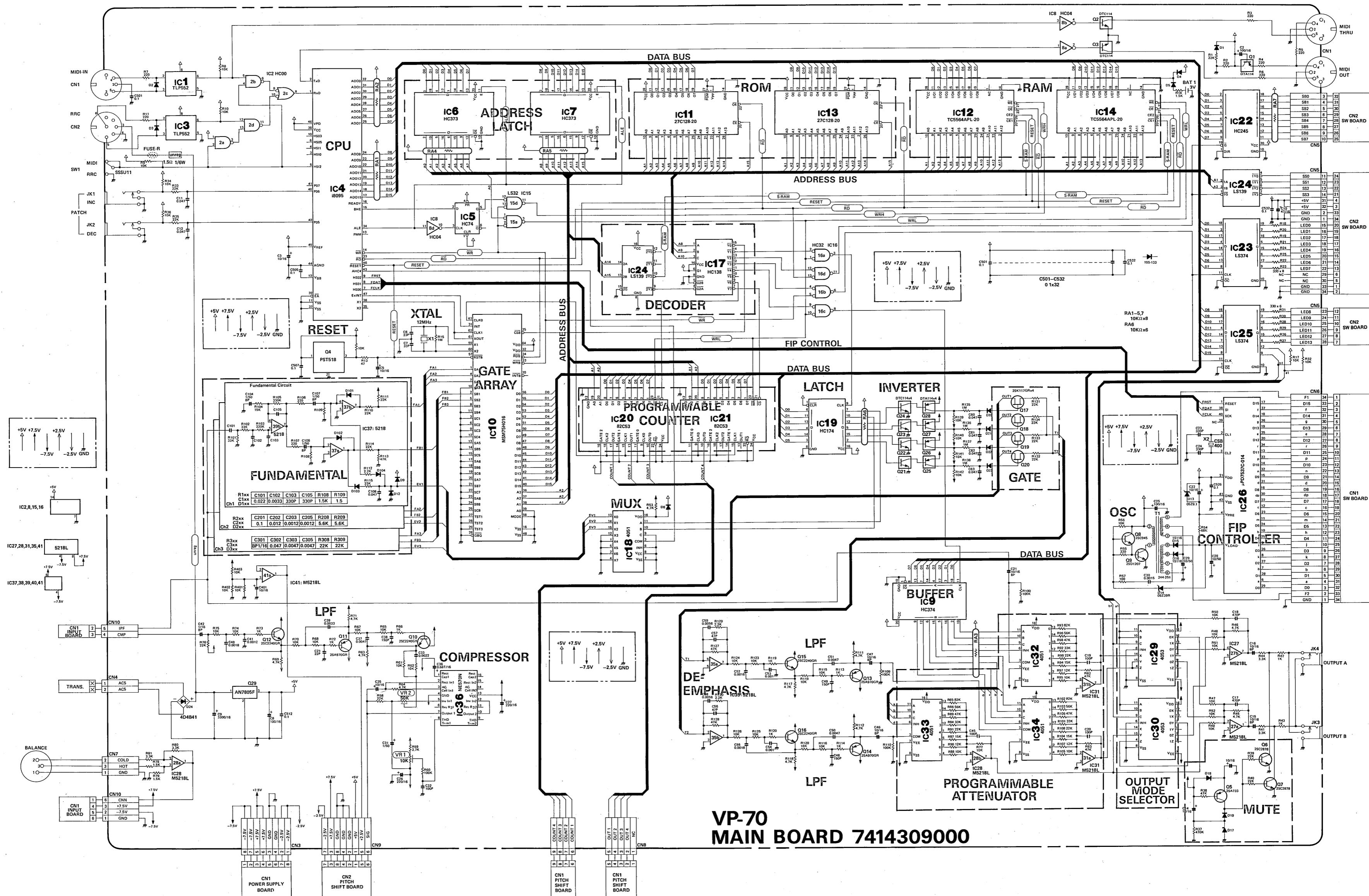
Lithiumparisto. Räjähdyssävaria.
Pariston saa vaihtaa ainoastaan
alan ammattimies.

Kun vaihat lithium pariston KÄYTÄ saman valmista-
jan samaa tyyppiä.



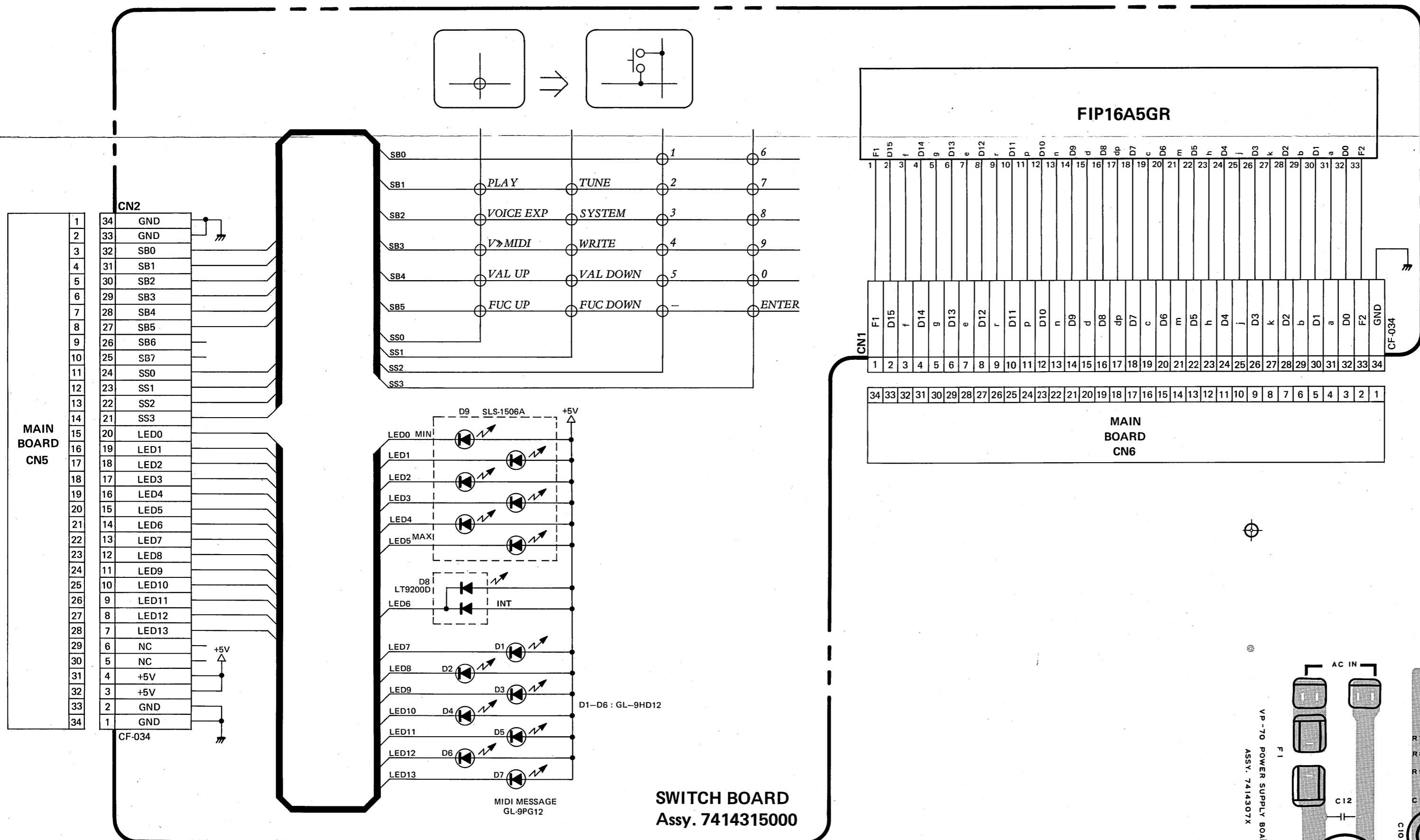
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49

CIRCUIT DIAGRAM

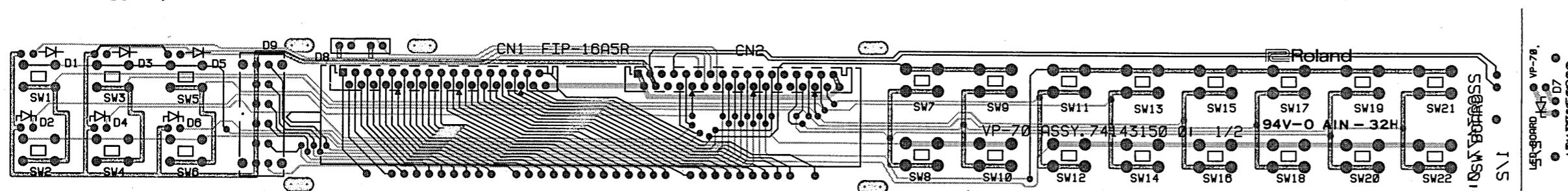
VP-70
MAIN BOARD 7414309000

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 4

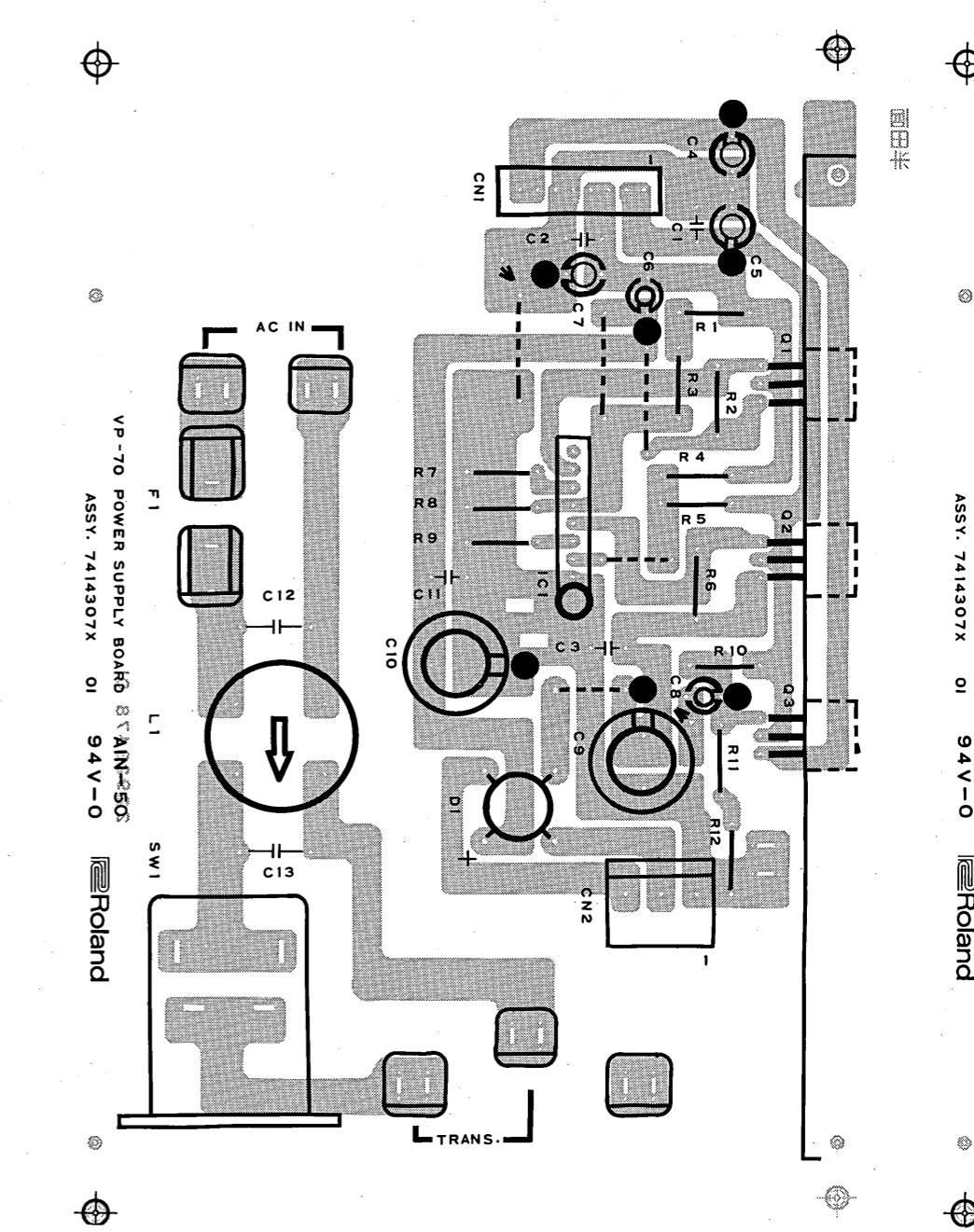
CIRCUIT DIAGRAM



SW BOARD w/LED BOARD ASSY 7414315001 (pcb 229234770)



View from component side

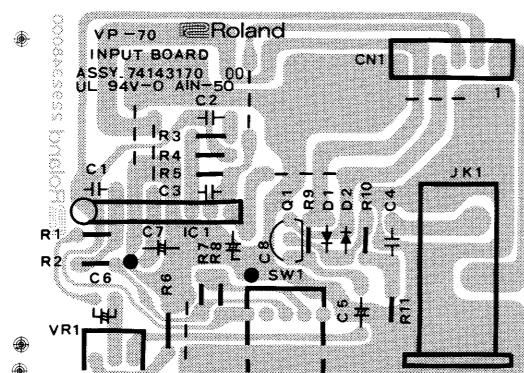


View from component side

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

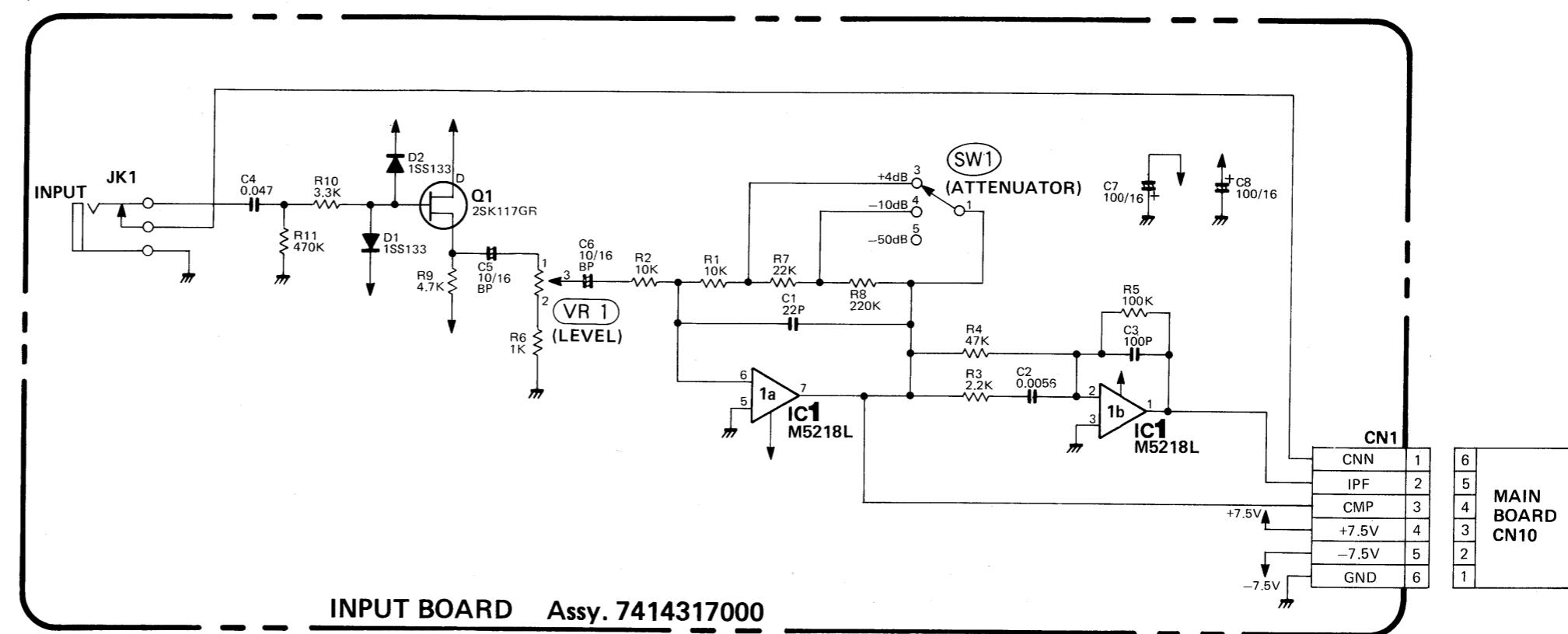
A B C D E F G H I J K L M N O P Q R S T U V

**INPUT BOARD
ASSY 741431700
(pcb 2292348000)**



View from component side

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM

